Conduction Loss

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Foreword

Modern scientific papers published all over the world play a major role in disseminating new ideas, concepts and innovations that have propelled the state of the art in technology to amazing heights in the last few decades. These papers, in my opinion, were missing one thing which is being interactive. That is, the ability of the reader to examine the raw data, the mathematical derivations of the formulae used in the paper and the ability to take a individualized look at the intermediate and final results. The Maple^{TM} document format provides all these features by allowing a single document to contain text, graphics, embedded objects and the best symbolic and numerical engine in the industry.

This paper/worksheet is an attempt to take advantage of all these features and uniquely allow the reader to explore a fresh view of the subject of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) conduction losses while giving him/her the opportunity to take a different look at the results obtained by the author while reading the detailed text of the paper. Feel free to generate different graphs or examine different packages or silicon by entering your own parameter set.

Abstract

As the PC makers push for DC-DC converters delivering >150 A at output voltages ≤1V within the next few years, the semiconductor manufacturers are pushing to optimize their MOSFET by improving both the silicon and the packages to provide switching devices suitable for these challenges. In this paper we will address the parasitic resistance attributed to the package alone and in isolation from the silicon on-resistance. We will show that in most of the traditional packages this resistance has a very strong frequency dependent component.

This means that at a switching frequency of about a few megahertz, this parasitic resistance will constitute a large percentage of the total device on-resistance and hence influences the losses greatly. Based on this observation, we will concentrate on the topology of choice, the synchronous buck converter, and we will derive conduction loss equations that are frequency dependent and calculate actual losses and examine several effects that follow.

Introduction

It is estimated that personal computers (PCs), notebook computers and servers annually use in excess of 500 million synchronous buck DC-DC converters each year. This number alone justifies an in-depth analysis of this very popular topology to enable engineers to refine their design process and save energy and help the environment at the same time. There are several loss mechanisms in this topology but, in this paper, we will concentrate on the conduction loss alone.

Traditionally, the conduction loss, Pc, in power MOSFETs has been calculated from the formula $Pc = I_L^2 \cdot R_{DSON} \cdot \Delta$ where I_L is the inductor current, R_{DSON} is the MOSFET's on-resistance plus the package parasitic resistance and Δ is the duty cycle. In this formula, the assumption is that the package parasitic resistance is a constant and is independent of frequency. However, a closer look at the package (see Figure 2) reveals that the bonding wires are thin enough with a diameters of few thousands of an inch that points towards possible skin effect influence on the parasitic resistance.

In this paper we explore the influence of skin effect on power MOSFET's parasitic resistance. Formulae will be derived to express the package parasitic resistance as a function of frequency and power loss will be calculated to demonstrate the percentage error that results if we do not take this effect into account.

Synchronous Buck Converter

Figure 1 depicts a simplified synchronous buck converter. This topology is the workhorse of the PC power conversion industry, which offers an excellent combination of simplicity of operation, ease of control, high conversion efficiency and the all-important low cost. We will concentrate on the conduction losses in both the M_{HS} and M_{LS} MOSFETs. The frequency effects of the dynamic losses will not be addressed in this paper. The switching current in both of these devices are a rectangular wave that that is represented in Figure 4.

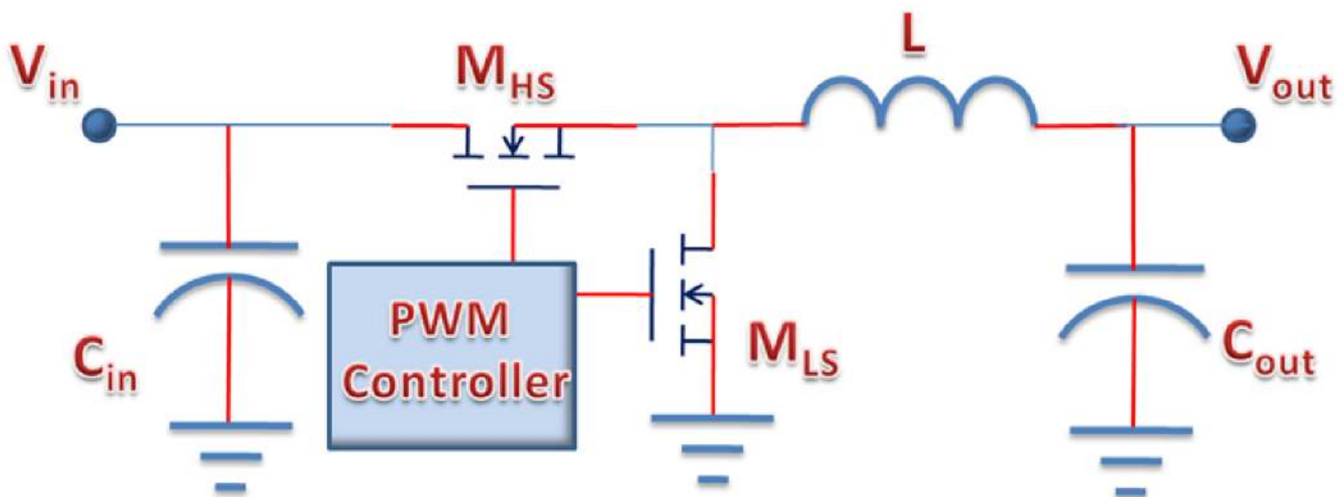


Figure 1. Synchronous Buck Converter

Principles of operation

Assume the lower MOSFET, M_{LS}, is initially turned OFF and the top or control MOSFET, M_{HS}, is turned ON. This applies the input voltage to one end of the inductor, causing the inductor current to ramp up. When M_{HS} is turned OFF, the current will continue to flow through the inductor but now it flows through M_{LS} body diode. After a dead time on the order of a few tens of nanoseconds—dictated by the PWM controller—the MOSFET M_{LS} turns ON. This allows all the inductor current to flow through M_{LS} rather than its body diode since the voltage drop across its on-resistance, R_{DSON} is lower than the diode voltage drop.

Assuming that the current through the inductor does not reach zero (the Continuous Conduction Mode or CCM), the voltage across the lower MOSFET will simply be $R_{DSON} \cdot I_L$ during the full OFF period of the top MOSFET where I_L is the inductor current.

At the end of the OFF period of the top MOSFET M_{HS}, the lower MOSFET, M_{LS}, will turn OFF, allowing the inductor current to flow in the body diode once more. After the dead time, the top MOSFET will turn ON and the cycle repeats. The average voltage at the output will depend on the average ON time of the top MOSFET if the inductor current is continuous. the output voltage V_{out} may be calculated from the equation $V_{out} = \Delta \cdot Vin$ where Δ is the duty cycle and is equal to $\frac{t_{on}}{T_S}$ where t_{on} is the on time of the control MOSFET and T_s is the duration of one cycle where $T_s = \frac{1}{f_s}$ where f_s is the converter switching frequency.
The conduction losses have traditionally been calculated from the equation $P_{conduction} = I_{load}^{2} \cdot \Delta \cdot \left(RDSON + R_{parasitics} \right)$ where all parameters are self explanatory. We will demonstrate that this equation, though useful as a rough estimate, may not be accurate enough for accurate analysis.

The switching currents in M_{HS} and M_{LS} are approximately of a rectangular shape. Using Fourier analysis one may break it down to its constituent sinusoidal currents of frequencies $n \cdot f_s$ where $n = 1 .. \infty$. Complete analysis is available later on in this worksheet.

Package Parasitic Resistance:

Due to the skin effect phenomenon, the bonding wires of the drain, gate and source leads exhibit different parasitic resistance at different frequencies.The package parasitic resistance is usually between 60 $\mu\Omega$ for advanced packages to about 2.2 $m\Omega$ for the SO8 package and mainly depends on the bonding wires' diameter and length and their physical proximity to each other. This is a very small value that may be ignored in other small signal applications but in modern power circuits, we will show that it represents an appreciable part of the total on-resistance of the switching device, which is the MOSFET for the purposes of this paper. To accurately determine the parasitic resistance it was important to isolate the package from the MOSFET silicon. To calculate the resistance as a function of frequency, we chose to employ finite element analysis (FEA) techniques.

This has the advantage of allowing us to determine very small resistance values without the need for

special test equipment and fixtures. It also eliminated any error which will be introduced by the test environment. A harmonic analysis was used to model the magnetic field surrounding the package. Resistance is then determined by extracting the real part of the characteristic impedance (Z_0).

Figure 2 shows both the SO8 and DPAK packages and all their constituents that affect the simulation. As can clearly be seen this is a fairly complex structure, which cannot readily yield a closed form function describing the parasitics. The approach we have taken was to fit a curve to the results of the finite element analysis performed at various frequencies. This curve then describes the parasitic resistance as a function of frequency. This is done so we can introduce this function in the loss equations which ultimately allows us to study the effect of this phenomenon on the predicted losses using DC on-resistance as it is performed today.

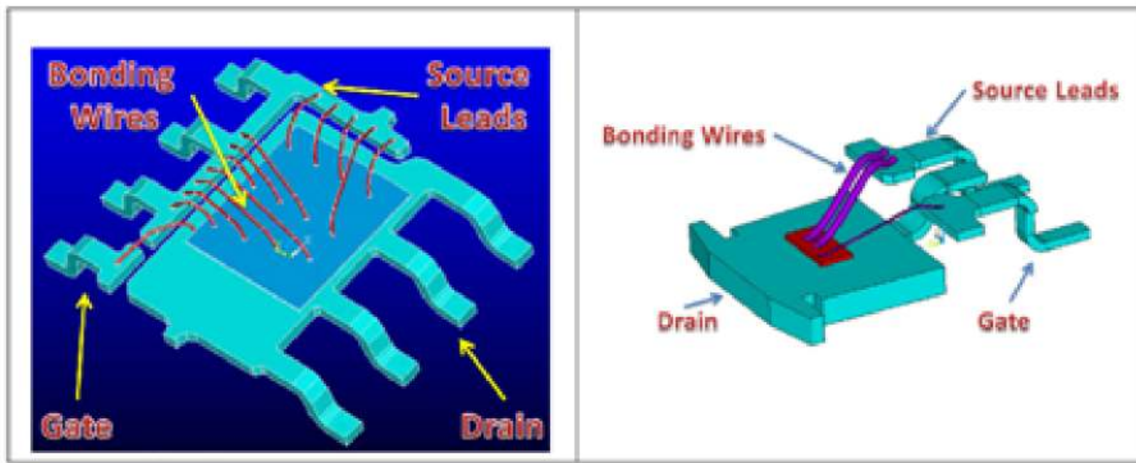


Figure 2. Finite element Models for SO8 (left) and DPAK (right) power package

Figure 3 shows several curves for each package. The first in black is the calculated value of the parasitic resistance using finite element analysis and the red, blue and green curves are the plots of the fit function for 2nd, 3rd and 4th orders. The fit functions for several packages will be derived later in this paper. We have chosen to extend the simulation to 100 MHz to account for close examination of the loss equations up to a very high harmonic number.

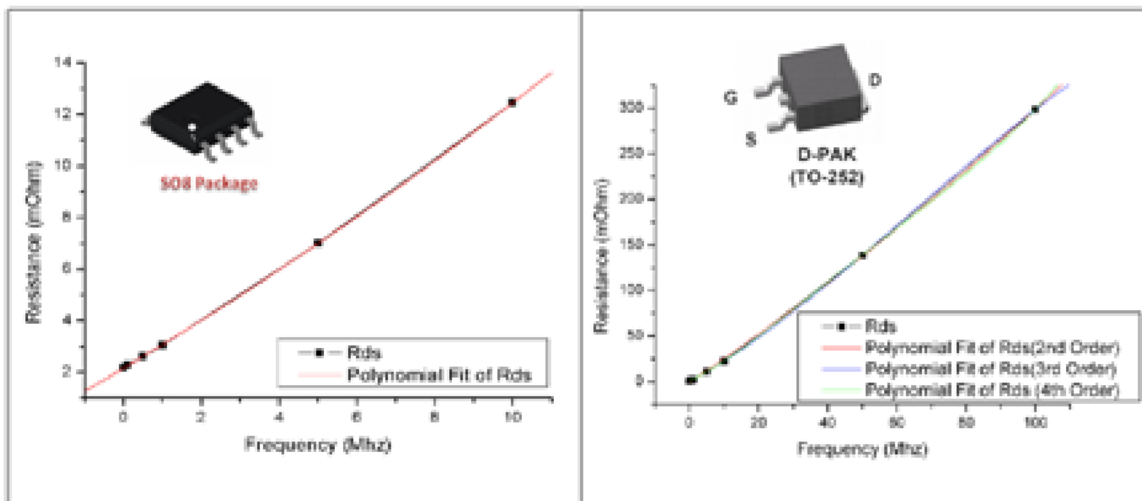


Figure 3. Parasitic Resistance as a function of frequency for SO8 (left) and DPAK (right)

Figure 3 shows this effect clearly. The value of R_{DS} goes up by a full order of magnitude by changing the switching frequency from 30 KHz to a mere 10 MHz. This effect is very significant in switching MOSFETs since the device's on-resistance R_{DSON} is in the range of a few $m\Omega$ to start with.

Switching Drain Currents

Input Parameters

$t_r := 10\cdot 10^{-9} : t_f := 10\cdot 10^{-9} : I_s := 15 : I_{pk} := 20 : \Delta := 0.2 : T_s := \frac{1}{f_s} : t_{on} := \Delta\cdot T_s :$

where t_r = current rise time, t_f = current fall time, I_{pk} =peak current, and I_s = the inductor current at the start of M_{HS} on time.

The switching current is shown in Figure 4.

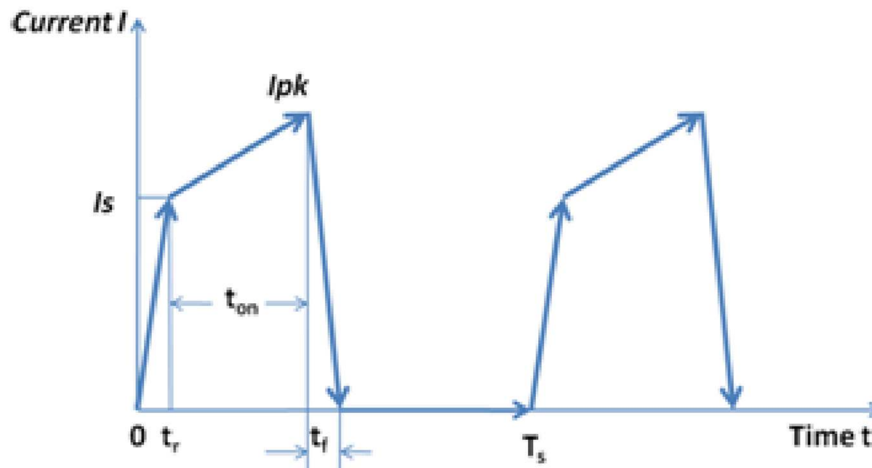


Figure 4. Switching Current Waveform

Each current cycle may be divided in four distinct regions as follows:

1. $t = 0\,..t_r$: the time for the MOSFET current to rise from $0[\![A]\!]$ to I_s.

2. $t = t_r..t_r + t_{on}$: the time duration of the M_{HS} switched fully on. During this time (the on-time) the inductor current ramps from I_s to I_{pk}.

3. $t = t_r + t_{on}\,..t_r + t_{on} + t_f$: when the M_{HS} is switched off, the MOSFET current starts falling from I_{pk} to $0[\![A]\!]$.

4. $t = t_r + t_{on} + t_f..T_s$: M_{HS} continues to be off while M_{LS} is turned on.

The first segment, $I1$, from $t = 0\,..t_r$ may be expressed as $I1 := \frac{I_s\cdot t}{t_r}$: .

The second segment, $I2$, is from $t = t_r .. t_r + t_{on}$ may be expressed as $I2 := I_s + \frac{(I_{pk} - I_s) \cdot t}{t_{on}}$: .

The third segment from $t = t_r + t_{on} .. t_r + t_{on} + t_f$ the drain current may be expressed as

$I3 := I_{pk} \cdot \left(1 - \frac{(t - (t_r + t_{on}))}{t_f}\right)$: .

The last segment, $I4$, from $t = t_r + t_{on} + t_f .. T_s$ and is $I4 := 0$: .

The Fourier series of a periodic function $f(x)$ with a period of $2l$ may be expressed in the form:

$FSf = a0 + \sum_{n=1}^{\infty} \left(an \cdot \cos\left(\frac{n \cdot \pi \cdot x}{l}\right) + bn \cdot \sin\left(\frac{n \cdot \pi \cdot x}{l}\right)\right)$: where a0 is the averaged current.

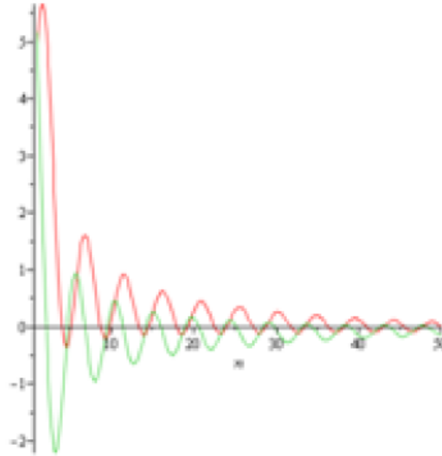
Now we can calculate the average current $a0$ as well as an and bn:

$$a0 := \frac{\left(\int_0^{t_r} \frac{I_s \cdot t}{t_r} \, dt + \int_{t_r}^{t_r + t_{on}} \left(I_s + \frac{(I_{pk} - I_s) \cdot t}{t_{on}} \right) dt + \int_{t_r + t_{on}}^{t_r + t_{on} + t_f} \left(I_{pk} \cdot \left(1 - \frac{(t - (t_r + t_{on}))}{t_f} \right) \right) dt \right)}{T_s} :$$

$$an := \frac{1}{\frac{T_s}{2}} \cdot \left(\int_0^{t_r} \frac{I_s \cdot t}{t_r} \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) dt + \int_{t_r}^{t_r + t_{on}} \left(I_s + \frac{(I_{pk} - I_s) \cdot t}{t_{on}} \right) \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) dt + \int_{t_r + t_{on}}^{t_r + t_{on} + t_f} \left(I_{pk} \cdot \left(1 - \left(\frac{t - (t_r + t_{on})}{t_f} \right) \right) \right) \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) dt \right) :$$

$$bn := \frac{1}{\frac{T_s}{2}} \cdot \left(\int_0^{t_r} \frac{I_s \cdot t}{t_r} \cdot \sin\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) dt + \int_{t_r}^{t_r + t_{on}} \left(I_s + \frac{(I_{pk} - I_s) \cdot t}{t_{on}} \right) \cdot \sin\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) dt + \int_{t_r + t_{on}}^{t_r + t_{on} + t_f} \left(I_{pk} \cdot \left(1 - \left(\frac{t - (t_r + t_{on})}{t_f} \right) \right) \right) \cdot \sin\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) dt \right) :$$

$plot\left(\left\{subs\left(f_s = 10^6, an\right), subs\left(f_s = 10^6, bn\right)\right\}, n = 1\,..\,50\right)$



By plotting both *an* and *bn* as a function of *n*, we can observe the envelope of the discrete values of both of them. The reason $n = 50$ was chosen is that the highest frequency we deal with here is 2 MHz and the 50th harmonic will be 100MHz which is the top value of frequency in our FEA.

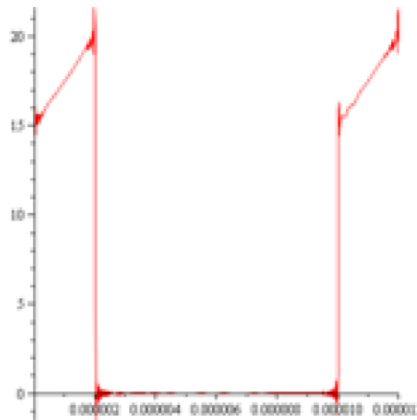
In this paper we will only consider the top MOSFET M_{HS}. This is because in PC applications the duty cycle is relatively small $\leqslant$ 12% resulting in a very rich harmonic content in the derived Fourier series for the switching current. The low side MOSFET M_{LS} has a duty cycle $\geqslant$ 87% resulting in low harmonics and significantly less harmonics.

Now we can express the switching current in the Fourier series, I_t, as:

$$\#I_t := a0 + \sum_{n=1}^{\infty} \left(an \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) + bn \cdot \sin\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) \right)$$

Now let us verify the above results by plotting the Fourier series representation of the switching current:

$$plot\left(subs\left(f_s = 10^5, \left(a0 + \sum_{n=1}^{200} \left(an \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) + bn \cdot \sin\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} \right) \right) \right) \right), t = 0\,..12 \cdot 10^{-6} \right)$$



As can be observed, it is the same as the waveform in Figure 4. One worthwhile observation is that the overshoot seen in the waveform is known as the **Gibbs phenomenon**, named after *Josiah Willard Gibbs,* the American mathematical physicist, as the phenomenon was noted by him in 1899. This overshoot appears in all Fourier series representation of any function with a jump similar to the above.

In order to calculate the losses, we must represent the term $an \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}}\right) + bn \cdot \sin\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}}\right)$

equivalently, in the form $An \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} + \Phi n\right)$, where the peak amplitude An and the phase Φn are

$An = \sqrt{an^2 + bn^2}$ and $\Phi n = \arctan\left(\frac{bn}{an}\right)$.

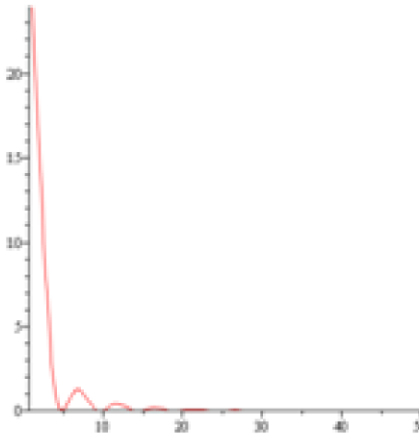
Since the phase value has no effect on power calculations, only *An* is is needed for our calculation.

The root mean square (RMS) value of the amplitude is $\frac{An}{\sqrt{2}} = \sqrt{\frac{an^2 + bn^2}{2}}$.

Now the switching current I_{ts}, may be written as:

$$\#Its := a0 + \sum_{n=1}^{\infty}\left(\sqrt{\frac{an^2 + bn^2}{2}} \cdot \cos\left(\frac{n \cdot \pi \cdot t}{\frac{T_s}{2}} + \arctan\left(\frac{bn}{an}\right)\right)\right)$$

$$plot\left(subs\left(f_s = 10^6, \frac{an^2 + bn^2}{2}\right), n = 1..50\right)$$



By plotting $\frac{an^2 + bn^2}{2}$ we can observe the envelope of the squared discrete current amplitudes.

The total MOSFET on-resistance, R_{DSON}, is made of two basic parameters:

1. The silicon on-resistance, R_{DS}.

2. Package parasitic resistance, R_P.

Thus, $R_{DSON} := R_{DS} + R_P$

The following are the Finite Element Analysis data for the SO8, DPAK and D2PAK packages:

$freq := [0, 0.1, 0.5, 1, 5, 10, 50, 100]$: where $freq$ is the frequency in megahertz.

$RPSO8 := [2.16, 2.28, 2.62, 3.05, 7.01, 12.46, 45.33, 68.01]$: the raw parasitic resistance data for the SO8 package in mΩ.

$RPDPAK := [0.528, 0.665, 1.421, 2.384, 11.000, 22.858, 138.796, 298.511]$: the raw parasitic resistance data for the DPAK package in mΩ.

$RPD2PAK := [0.995, 1.242, 2.714, 4.849, 23.001, 43.186, 237.825, 508.887]$: the raw parasitic resistance data for the D2PAK package in mΩ.

Using the **Curve Fitting Assistant** in Maple, we can fit curves for the parasitic resistance as a function of the frequency, F, in megahertz, and the parasitic resistance in mΩ.

$$RPSO8 := 2.16 + \cfrac{F}{0.8333333333 + \cfrac{F - 0.1}{1.577142858 + \cfrac{F - 0.5}{0.3936605317 + \cfrac{F - 1}{-20.01286710 + \cfrac{F - 5}{-0.3384392972 + \cfrac{F - 10}{143.4580373 + 0.04879329924 \cdot F}}}}}} :$$

$$RPDPAK := 0.528 + \cfrac{F}{0.7299270073 + \cfrac{F - 0.1}{-2.352711538 + \cfrac{F - 0.5}{-0.2122214782 + \cfrac{F - 1}{-77.49758132 + \cfrac{F - 5}{-0.1316186986 + \cfrac{F - 10}{-40.7422033 - 11.60142864 \cdot F}}}}}} :$$

$$RPD2PAK := 0.995 + \cfrac{F}{0.4048582996 + \cfrac{F - 0.1}{-3.509033057 + \cfrac{F - 0.5}{-0.1864756513 + \cfrac{F - 1}{-8878.371139 + \cfrac{F - 5}{0.0005280184 + \cfrac{F - 10}{1275.433328 + 30.12693717 \cdot F}}}}}} :$$

Each formula has a DC term and several frequency dependent terms. One further point: in this analysis, the minimum skin frequency is approximately 30 KHz for the packages used; below this frequency the skin effect may be considered zero. Therefore, these equations should be used to calculate the parasitic resistance for the frequency F, where $0.03\ [\![MHz]\!] \le F \le 100 [\![MHz]\!]$. The DC value of the parasitic resistance is taken directly from the raw data. $F = n \cdot f_s$ where n is the harmonic number and f_s is the DC-DC converter's switching frequency.

Now we can write the equation for the packaged MOSFET on-resistance:

$R_{DSON} = R_p + R_{DS}$ where R_p is as before and R_{DS} is the silicon on-resistance.

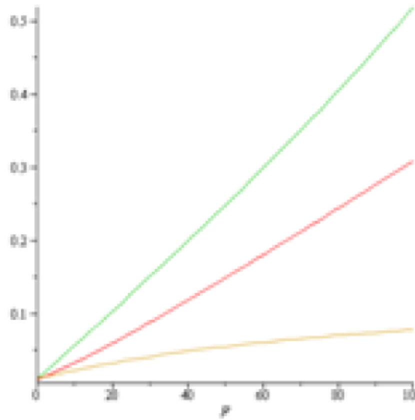
$\therefore$ The equations for R_{DSON} for all the packages under consideration can be written as:

$$RDSONSO8 := RPSO8 \cdot 10^{-3} + R_{DS}:$$

$$RDSONDPAK := RPDPAK \cdot 10^{-3} + R_{DS}:$$

$$RDSOND2PAK := RPD2PAK \cdot 10^{-3} + R_{DS}:$$

$$plot(\{subs(R_{DS} = 0.01,\ RDSOND2PAK), subs(R_{DS} = 0.01,\ RDSONDPAK), subs(R_{DS} = 0.01,\ RDSONSO8)\}, F = 0..100)$$



The above graph shows the parasitic resistance as a function of frequency for all three packages. Notice that the parasitic resistance can go as high as 500 $m\Omega$ at 100MHz for bonding wires of only 1 $m\Omega$ when measured at DC.

$\therefore$ the total power dissipation may be written as:

$$PtotSO8 := a0^2 \cdot subs(F = 0, RDSONSO8) + \sum_{n=1}^{50} \left(\left(\sqrt{\frac{an^2 + bn^2}{2}} \right)^2 subs\left(F = \frac{n \cdot f_s}{10^6}, RDSONSO8 \right) \right):$$

$$PtotDPAK := a0^2 \cdot subs(F = 0, RDSONDPAK) + \sum_{n=1}^{50} \left(\left(\sqrt{\frac{an^2 + bn^2}{2}} \right)^2 subs\left(F = \frac{n \cdot f_s}{10^6}, RDSONDPAK \right) \right):$$

$$PtotD2PAK := a0^2 \cdot subs(F = 0, RDSOND2PAK) + \sum_{n=1}^{50} \left(\left(\sqrt{\frac{an^2 + bn^2}{2}} \right)^2 subs\left(F = \frac{n \cdot f_s}{10^6}, \right.\right.$$

$$RDSOND2PAK\Big)\Big) :$$

We have replaced ∞ by 50 to facilitate graphing and calculations with reliable accuracy.

The traditional conduction loss calculations can be written as follows:

1. Calculate the RMS value of the current, I_{SRMS}, first:

$$I_{SRMS} := \left(\frac{1}{T_s}\left(\int_0^{t_r}\left(\frac{I_s \cdot t}{t_r}\right)^2 dt + \int_{t_r}^{t_r+t_{on}}\left(I_s + \frac{(I_{pk}-I_s)\cdot t}{t_{on}}\right)^2 dt + \int_{t_r+t_{on}}^{t_r+t_{on}+t_f}\left(I_{pk}\cdot\left(1 - \frac{(t-(t_r+t_{on}))}{t_f}\right)\right)^2 dt\right)\right)^{1/2} :$$

2. Calculate the traditional conduction loss, *Pcref*:

$$Pcref := I_{SRMS}^2 \cdot (R_{DS} + R_P) :$$

Now we can derive a formula of the error using the traditional value vs. that using the frequency dependent parasitic resistance.

$$PercentErso8 := \frac{PtotSO8 - subs(R_P = 0.00216, Pcref)}{subs(R_P = 0.00216, Pcref)} \cdot 100 :$$

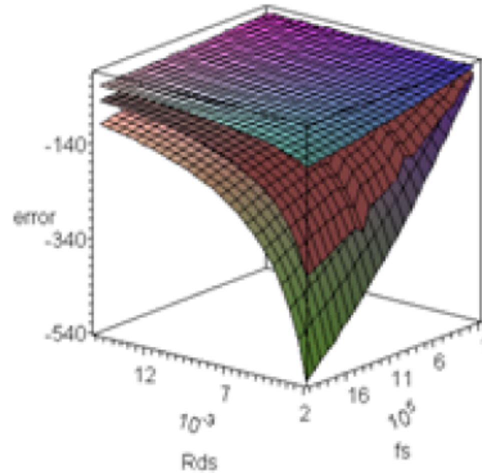
$$PercentErDPAK := \frac{PtotDPAK - subs(R_p = 0.000528, Pcref)}{subs(R_P = 0.000528, Pcref)} \cdot 100 :$$

$$PercentErD2PAK := \frac{PtotD2PAK - subs(R_P = 0.000995, Pcref)}{subs(R_P = 0.000995, Pcref)} \cdot 100 :$$

$$plot3d\left(\left\{\frac{subs(R_P = 0.000995\ , Pcref - PtotD2PAK)}{subs(R_P = 0.000995\ , Pcref)} \cdot 100, \frac{subs(R_P = 0.000528, Pcref - PtotDPAK)}{subs(R_P = 0.000528\ , Pcref)}\right.\right.$$

$$\cdot 100\,,\ \frac{subs\left(R_P = 0.00216\ ,\ Pcref - PtotSO8\right)}{subs\left(R_P = 0.00216\ ,\ Pcref\right)} \cdot 100 \Big\}, R_{DS} = 0.002\ ..0.015, f_s = 10^5\ ..2 \cdot 10^6, axes$$

$$= boxed\Big)$$

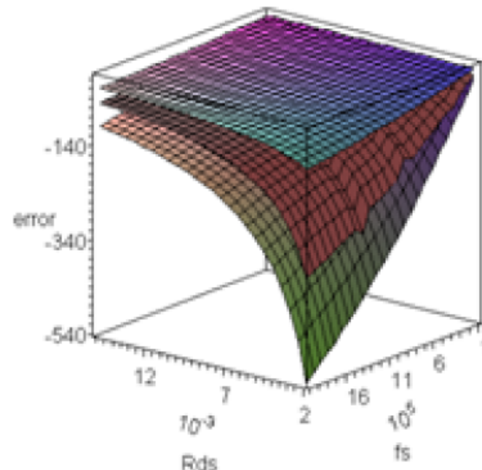


The percentage error (z-axes) as a function of the switching frequency
and the silicon on-resistance for SO8, DPAK and D2PAK Package

The above graph depicts the percentage error between the calculation using the traditional formula vs. using the formulae derived above with skin effect taken into consideration.

Please notice that D2PAK will deliver 540% error when operating at 2 MHz and 2 mΩ on-resistance. It is also worth noting that at a very low switching frequency, where fs ≤ 100 KHz, there is a negligible increase in parasitic resistance due to skin effect.

$$plot3d\left(\left\{\frac{PtotD2PAK}{subs\left(R_P = 0.000995\ ,\ Pcref\right)} \cdot 100, \frac{PtotDPAK}{subs\left(R_P = 0.000528\ ,\ Pcref\right)} \cdot 100, \frac{PtotSO8}{subs\left(R_P = 0.00216\ ,\ Pcref\right)} \cdot 100\right\}, R_{DS} = 0.002\ ..0.015, f_s = 1E5\ ..2E6, axes = boxed\right)$$



The ratio $\frac{Conduction\ loss\ using\ skin\ effect\ contribution}{conduction\ loss\ using\ traditional\ equations}$ (z axis)

The above graph shows that in order to have efficient high frequency converters, designers must use advanced packages or they risk having inefficient power conversion leading to unacceptable power losses.

Conclusion

1. The package parasitic resistance represents an appreciable part of the MOSFET on-resistance in power applications.
2. The package parasitic resistance possesses a very strong frequency dependence due to the skin effect phenomenon.
3. A higher fundamental switching frequency will result in higher parasitic resistance and hence higher conduction losses.
4. The DC conduction losses calculated above produce an error that can be as large as 500% depending on the package and the fundamental switching frequency.
5. When choosing the switching frequency for a given application, it is mandatory to examine this above mentioned effect to weigh the pros and cons of such a selection.
6. New packages have been developed by several manufacturers that address this problem with varying degrees of success. Some are very successful like DirectFet BGA.
7. As the DC-DC converters are expected to perform at higher efficiencies, particularly in the notebook field, all loss mechanisms must be placed under the microscope in an attempt to minimize their effect and provide the overall solution that fully utilizes all the advantages made so far in MOSFET design.
8. Both with breakthroughs in silicon and in innovative packaging, these new switching devices continue to deliver improvement in performance at very reasonable prices .

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